IN THE CLAIMS

Please amend Claim 1 as follows.

1. **(Currently Amended)** In a system in which an ATM slave processing unit is coupled to an ATM master processing unit by a communication bus, the interaction between the ATM master processing unit and the ATM slave processing unit having a UTOPIA format, ~~An~~ an ATM slave interface unit providing an interface between ~~an ATM master processing unit~~ the communication bus and a direct memory access unit coupled to an ATM slave processing unit, the interface unit comprising:

an input unit, the input unit receiving data cells and exchanging control signals with the ATM master processing unit;

an input buffer unit receiving data signals and exchanging control signals with the input unit, the input buffer unit including:

a buffer storage unit coupled to the input unit, the buffer storage unit being a two-stage, first-in/first-out memory unit, the buffer storage unit storing received data cells, the buffer storage unit transferring data cells to the direct memory access unit in response to a first READY signal; and

a calculation unit, ~~wherein the input buffer unit receives data signals from and exchanges control signals with the input unit, the input buffer unit storing received data cells in the buffer storage unit, the buffer storage~~

~~unit transferring data cells to the direct memory access unit~~; and

a register, each data cell including a cell portion having an encoded destination location, the calculation unit responsive to the contents of the register and to the cell portion for generating a destination location for the data cell in the ATM slave processing unit; and

an output unit, the output unit including;

an output buffer storage unit, the output buffer unit being a two-stage first-in first-out storage unit for storing data cells, the output buffer unit receiving data cells from the direct memory access unit in response to a second READY signal, the data buffer unit exchanging control signals with the direct memory access unit; and

an output unit, the output unit receiving data cells from the output buffer unit and applying data cells to the communication bus, the output unit exchanging control signals with the ATM master processing unit.

Please cancel Claim 2.

2. **(Currently Cancelled)** ~~The interface unit as recited in claim 1 wherein the buffer storage unit is a first-in/first-out memory unit.~~

Please cancel Claim 3.

3. **(Currently Cancelled)** ~~The interface unit as recited in claim 2 wherein the first-in/first-out memory unit can store at least two data cells.~~

4. **(Original)** The interface unit as recited in claim 1 wherein the buffer storage unit transfers a data cell to the slave data processing unit every clock cycle.

Please amend Claim 5 as follows.

5. **(Currently Amended)** The interface unit as recited in claim 1 wherein the destination locations ~~can be~~ are selected from at least one of the group consisting of a slave processing unit, a shared memory location for a plurality of slave processing units, and at least one slave processing unit and at least one shared memory location.

Please cancel Claim 6.

6. **(Currently Cancelled)** ~~The interface unit as recited in claim 1 further comprising:~~

~~an output buffer unit; the output buffer unit including a buffer storage unit, the buffer unit storing data cells, the output buffer unit receiving data cells from the direct memory access unit the data buffer unit exchanging control signals with the slave processing direct memory access unit; and~~

~~an output unit; the output unit receiving data cells from the output buffer unit and applying data cells to the ATM master processing unit, the output unit exchanging~~

~~control signals with the output buffer unit and with the ATM master processing unit.~~

7. **(Original)** The interface unit as recited in claim 1 wherein the ATM slave processing unit includes at least one digital signal central processing unit.

Please cancel Claim 8.

8. **(Currently Cancelled)** ~~The interface unit as recited in claim 1 wherein the control signals and the data cells have a UTOPIA format.~~

9. **(Cancelled)**

Please amend claim 10 as follows.

10. **(Currently Amended)** A method for exchanging data cells from an ATM master processing unit with a plurality of locations in an ATM slave processing unit over a communication bus, the ATM slave processing unit including a direct memory access unit, the method comprising:

storing data cells from the ATM master processing unit in a buffer storage unit coupled to the communication bus, wherein the buffer storage unit is a two-stage, first-in/first-out storage unit;

comparing a field in the data cell with the contents of a register to determine the destination location of ~~the~~ each data cell;

generating a signal identifying the destination location; and

when storage space is available, transferring a data cell from the buffer storage unit to the direct memory access unit in response to READY signal.

Please amend Claim 11 as follows.

11. **(Currently Amended)** The method as recited in claim 10 further comprising:

~~implementing the buffer storage to hold two data cells; and~~

transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive clock cycles.

Please amend Claim 12 as follows.

12. (**Currently Amended**) The method as recited in claim 11 further comprising implementing the ~~control~~ signals exchanged ~~with the ATM master processing unit~~ over the communication bus in a UTOPIA format.

13. (**Previously Amended**) The method as recited in claim 10 wherein the method includes applying the signal identifying the destination location to the direct memory access unit.

Please amend Claim 14 as follows.

14. (**Currently Amended**) A data processing system comprising:

an ATM master processing unit;

a communication bus coupled to the ATM master processing unit;

an ATM slave processing unit, the ATM slave processing unit including a direct memory access unit; and

an ATM slave interface unit coupled to the communication bus, the slave interface unit including:

an input unit, the input unit ~~receiving data signals from~~ exchanging UTOPIA format signal with the ATM master processing unit~~, the input unit exchanging control signals with the ATM master unit~~;

an input buffer storage unit, the input buffer unit receiving data cell signals from the input unit, the input buffer unit including:

a memory unit, the memory unit being a two-stage, first-in/first-out storage unit; and

a calculation unit, ~~wherein the input buffer unit exchanges control signals with the input unit,~~ the input buffer unit storing data cells in the memory unit, the buffer storage unit transferring data cells to the ~~ATM slave processing unit~~ direct memory access unit, the input buffer unit ~~exchanging control signals with~~ transferring data cells to the direct memory access unit in response to READY signals; and

a register, the contents of the register identifying the destination location field in a data cell, the contents of the register providing the translation of a field in the data cell into a destination location, wherein the calculation unit generates a destination location signal and applies the destination location signal to the ~~ATM slave processing unit~~ direct memory access unit.

15. **(Cancelled)**

Please cancel Claim 16.

16. **(Currently Cancelled)** ~~The data processing system as recited in claim 14 wherein the memory unit is a first-in/first-out memory unit capable of storing at least two data cells.~~

Please cancel Claim 17.

~~17.~~ **(Currently Cancelled)** ~~The data processing system as recited in claim 16 wherein the input buffer unit transfers data cells to the ATM slave processing unit on consecutive clock cycles.~~